

WHAT IS CLAIMED IS:

1. A data input/output buffer, comprising:  
a plurality of switching elements and a plurality of logical elements,  
wherein an NMOS transistor of a switching element driven according  
5 to a data signal inputted from a peripheral circuit or a logical element to  
which the data signal is inputted, of the plurality of the switching elements or  
the plurality of the logical elements, is a low voltage-driven NMOS transistor.

2. The data input/output buffer as claimed in claim 1, wherein a  
10 threshold voltage of the low voltage-driven NMOS transistor is 0V.

3. The data input/output buffer as claimed in claim 2, further  
comprising a switching element that is turned on according to an output enable  
signal only when a data is outputted between the low voltage-driven NMOS  
15 transistor and a ground voltage terminal.

4. The data input/output buffer as claimed in claim 3, wherein the  
switching element is an NMOS transistor.

20 5. A data input/output buffer, comprising:  
a first logical element driven according to a data signal inputted from  
a peripheral circuit, the first logical element having a PMOS transistor and a  
low voltage-driven NMOS transistor; and

a second logical element for latching an output signal of the first logical element.

6. The data input/output buffer as claimed in claim 5, wherein a  
5 threshold voltage of the low voltage-driven NMOS transistor is 0V.

7. The data input/output buffer as claimed in claim 6, further  
comprising a switching element that is turned on according to an output enable  
signal only when a data is outputted between the low voltage-driven NMOS  
10 transistor and a ground voltage terminal.

8. The data input/output buffer as claimed in claim 7, wherein the  
switching element is an NMOS transistor.

15 9. A semiconductor memory device, comprising:  
a memory cell array;  
a row decoder for selecting a given page of the memory cell array  
according to a row address signal;  
a page buffer for storing data stored at the page selected by the row  
20 decoder;  
a column decoder for generating a bit line select signal according to a  
column address signal;  
a column multiplexer for selecting and outputting any one of the data  
stored at the page buffer according to the bit line select signal; and

a data input/output buffer for storing the data selected by the column multiplexer and transferring the data to a data line, wherein a device driven by the data is a low voltage-driven NMOS transistor.

5           10. The semiconductor memory device as claimed in claim 9, wherein a threshold voltage of the low voltage-driven NMOS transistor is 0V.

11. The semiconductor memory device as claimed in claim 10, further comprising a switching element that is turned on only when a data is outputted  
10 between the low voltage-driven NMOS transistor and a ground voltage terminal.

12. The semiconductor memory device as claimed in claim 11, wherein the switching element is an NMOS transistor.

15           13. The semiconductor memory device as claimed in claim 9, wherein the data input/output buffer comprises:

          a PMOS transistor driven according to the data signal outputted from the column multiplexer and connected to a power supply voltage terminal;  
20           a low voltage-driven NMOS transistor driven according to the data signal outputted from the column multiplexer and connected to the PMOS transistor;

a switching element connected between the low voltage-driven NMOS transistor and a ground voltage terminal, wherein the switching element is turned on only in a data output period; and

a latch unit for inverting and restoring a signal received via the PMOS  
5 transistor or the low voltage-driven NMOS transistor.

14. The semiconductor memory device as claimed in claim 13,  
wherein the switching element is an NMOS transistor.